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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/617,802	HSIEH, HSIANG-AN
	Examiner	Art Unit
	Ryan M. Stiglic	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending and have been examined.

2. Claims 1-8 are rejected.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "the microcontroller further comprises: buffer unit; power convert circuit; and stored program code" and "a first bus interface is provided in the microcontroller" must be shown or the feature(s) canceled from the claim(s). Figure 1 instead shows the claimed limitations [buffer unit and power convert unit] external to the microcontroller. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1 and 7 are objected to because of the following informalities: Claims 1 and 7 fail to follow the guidelines established by 37 C.F.R. §1.75 and MPEP § 608.01(i)-(p) [specifically 608.01(m)] in that the indicated claims contain a plurality of periods. MPEP § 608.01(m) recites, "Each claim begins with a capital letter and ends with a period. Periods may not be used elsewhere in the claims except for abbreviations." Appropriate correction is required.

5. Claim 7 objected to because of the following informalities: It is believed applicant intended "broad" to be spelled as "broad" and the Examiner will treat claim 7 as such. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. With regards to the 37 C.F.R. §1.75 claim objection above it is unclear what coverage the applicant wishes to seek in claims 1 and 7. In order to advance the prosecution of the instant application the Examiner has interpreted claims 1 and 7 as having all the limitations of sentence 1, further comprising "a second bus interface circuit and an interface detecting control and switching circuit which has the function of allowing the microcontroller to automatically detect and determine if the system supports either the first transfer interface or the second transfer interface so that data can be stored and read in the erasable memory media." Applicant is advised to amend claims 1 and 7 such that the recited claims possess only one period and a compilation of all the limitations previously set forth in the two separate sentences.

8. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 contains what is believed to be a key limitation within parenthesis. The Examiner respectfully submits that placing "standard MS transfer interface" and "MS bus interface" in parenthesis is not a positive recitation of the intended limitation, therefore it is unclear what the applicant regards has their invention. In order to advance prosecution of the instant application the Examiner has interpreted claim 2 as, "...of claim 1 wherein the first transfer interface is a standard MS transfer interface; the first bus interface circuit is a MS bus interface circuit; the microcontroller further comprises: buffer unit; power convert circuit; and stored program code." The Examiner advises applicant to follow a similar guideline when amending claim 2 such that it is clear what the applicant claims as their invention. Furthermore, the Examiner believes that as presented, "data transfer temporary store buffer unit and power convert circuit, control store and read interface, program code store memory media are set inside

in the microcontroller" is indefinite because it is unclear what the applicant regards as his/her invention.

9. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 recites the limitation "another second bus interface circuit" in page 8, lines 7-8. There is insufficient antecedent basis for this limitation in the claim. Claim 2 previously recites "a second transfer interface" instead of "a second bus interface" that would warrant the term "another"

10. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 recites the limitation "another USB bus interface" in page 9, line 6. There is insufficient antecedent basis for this limitation in the claim. Claim 8 previously recites "a USB transfer interface" instead of "a USB bus interface" that would warrant the term "another"

11. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 recites the limitation "wherein the another data transfer temporary store buffer unit, power converting circuit, control store and read interface, and program code store memory media are provided in the microcontroller" in page 9, lines 13-16. There is insufficient antecedent basis for this limitation in the claim.

12. Claims 2 and 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. Claims 2 and 8 recite the limitation "...in the converting device" in page 8, line 7 and page 9, line 5. There is insufficient antecedent basis for this limitation in the claim.

13. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

14. Claims 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The distinction between "second transfer interface" and "second bus interface" is indefinite because the two are used interchangeably in claim 4 ("second transfer interface is a USB ***bus*** interface").

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yao (6385677).

For claim 1 Yao discloses:

A MS (col. 4, ll. 30-36) silicon card with bi-interface comprising: a silicon card and its converting device, wherein the silicon card has

- a first transfer interface (Fig. 1, 102; col. 2, ll. 45-57; Fig. 3, "Host Interface 143"; col. 3, ll. 6-10) and
- circuit broad having
    - microcontroller (Fig. 1-2, 10) and erasable memory media (Fig. 1-2, 20),
    - a first bus interface is provided in the microcontroller (Fig. 2, 14; col. 2, ll. 58-63),
    - a slot for receiving the silicon card (Fig. 3, 30; col. 3, ll. 33-48) and
    - a second transfer interface for connecting with peripheral device (Fig. 1, 101; col. 2, ll. 45-57; Fig. 3, 133; col. 3, ll. 1-5) are provided in the converting device (Fig. 4).
- another second bus interface circuit (Fig. 2, 13; col. 2, ll. 58-63) and
- an interface detecting control and switching circuit are provided in the microcontroller of the silicon card, the interface detecting control and switching circuit has the function of allowing the microcontroller to automatically detect and determine that if the system supports either the first transfer interface or the second transfer interface so that the data can be stored and read in the erasable memory media (col. 3, ll. 12-26).

For claim 3 Yao discloses:

The MS silicon card with bi-interface of claim 1 wherein the second transfer interface is a USB transfer interface (Fig. 1, 102; col. 2, ll. 45-57; Fig. 3, "Host Interface 143"; col. 3, ll. 6-10).

For claim 4 Yao discloses:

The MS silicon card with bi-interface of claim 1 wherein the second transfer interface is a USB bus interface (Fig. 2, 14; col. 2, ll. 58-63).

For claim 5 Yao discloses:

The MS silicon card with bi-interface of claim 1 wherein the slot of the converting device is designed to have the structure of silicon card interface in order to provide the insertion for the silicon card (Fig. 3; col. 3, ll. 33-48).

For claim 6 Yao discloses:

The MS silicon card with bi-interface of claim 1 wherein the silicon card has at least two different system interface circuits includes the signal ports of CLK, SCLK, SDIO, Reserved 1, Reserved 2 with different functions (As previously discussed, Yao states the host interface adheres to the MS specification (col. 4, ll. 30-36), which as the applicant is aware contains CLK, SCLK, SDIO, Reserved 1, and Reversed 2 signal ports/pins.).

For claim 7 Yao discloses:

A MS silicon card (col. 4, ll. 30-36) with bi-interface comprising: a silicon card and its converting device, wherein the silicon card has a

- MS transfer interface (Fig. 1, 102; col. 2, ll. 45-57; Fig. 3, "Host Interface 143"; col. 3, ll. 6-10; col. 4, ll. 30-36) and
- circuit board with microcontroller (Fig. 1-2, 10) and erasable memory media (Fig. 1-2, 20),
- MS bus interface is provided in the microcontroller (Fig. 2, 14; col. 2, ll. 58-63; col. 4, ll. 30-36),
- a slot for receiving the MS silicon card (Fig. 3, 30; col. 3, ll. 33-48) and a
- USB transfer interface for connecting with peripheral device (Fig. 1, 101; col. 2, ll. 45-57; Fig. 3, 133; col. 3, ll. 1-5) are provided in the converting device (Fig. 4).
- another USB bus interface circuit (Fig. 2, 13; col. 2, ll. 58-63) and
- a interface detecting control and switching circuit are provided in the microcontroller of the MS silicon card, the interface detecting control and switching circuit has the function of allowing the microcontroller to automatically detect and determine that if the system supports either the MS transfer interface or the USB transfer interface so that the data can be stored and read in the erasable memory media (col. 3, ll. 12-26).

17. Claims 1, 3-5 rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. (US 20030212848A1).

For claim 1 Liu discloses:

A silicon card with bi-interface comprising: a silicon card and its converting device, wherein the silicon card has

- a first transfer interface (Fig. 1, 14; [0020]) and
- circuit broad having
  - microcontroller (Fig. 1, 22; [0020]) and erasable memory media (Fig. 1, 16; [0020]),
  - a first bus interface is provided in the microcontroller (Fig. 1, 28; [0021]),
  - a slot for receiving the silicon card ([0032] describes the process completed when the Flash memory card (Fig. 1, 10) is inserted into the appropriate slot) and
  - a second transfer interface for connecting with peripheral device (Fig. 1, 12; [0020]) are provided in the converting device).
- another second bus interface circuit (Fig. 1, 30; [0022]) and

an interface detecting control and switching circuit are provided in the microcontroller of the silicon card, the interface detecting control and switching circuit has the function of allowing the microcontroller to automatically detect and determine that if the system supports either the first transfer interface or the second transfer interface so that the data can be stored and read in the erasable memory media (Fig. 1, 20; [0024-0030]).

For claim 3 Liu discloses:

The MS silicon card with bi-interface of claim 1 wherein the second transfer interface is a USB transfer interface (Fig. 1, 12; [0020]).

For claim 4 Liu discloses:

The MS silicon card with bi-interface of claim 1 wherein the second transfer interface is a USB bus interface (Fig. 1, 30; [0020]).

For claim 5 Liu discloses:

The MS silicon card with bi-interface of claim 1 wherein the slot of the converting device is designed to have the structure of silicon card interface in order to provide the insertion for the silicon card ([0032] describes the process completed when the Flash memory card (Fig. 1, 10) is inserted into the appropriate slot).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao as applied to claims 1 and 7 above, and further in view of Spencer (6712277).

Yao teaches a dual interface memory card having both MS and USB interfaces. The memory card contains a microcontroller for controlling the sending and receiving of data, including the controlling of circuit connections with respect to the flash memory. Yao further teaches the MS silicon card with bi-interface of claim 1 wherein the silicon card has the first transfer interface (standard MS transfer interface) (Fig. 1, 102; col. 4, ll. 30-36), and at least the first bus interface

circuit (MS bus interface) (Fig. 2, 14; col. 4, ll. 30-36), data transfer temporary store buffer (The buffer unit of Yao is an inherent feature of the invention because the specification discusses the transfer of data to/from the memory card is performed at high-speed [col. 4, ll. 15-24]. Therefore some inherent buffer means is taught for temporarily storing data passed between the high-speed USB interface and the low-speed memory) unit and control store and read interface, program code store memory media are set inside in the microcontroller ("associated firmware" col. 2, ll. 61-63). While Yao teaches a USB interface receives a supply voltage (Fig. 1, 101), Yao does not teach a power convert circuit for dissipating the USB supply voltage.

Spencer teaches of a multiple interface memory card for use in a device with a compact flash interface (like that of Yao) or a system that communicates via a contact-less means, such as a RF communication system. The disclosure of Spencer teaches of memory card controller (Fig. 1, item 50) used to route data from either interface to the mass storage area(i.e. memory; Fig. 1, item 20). Each interface block performs the task of interface detection while the memory card controller selects an interface. Each interface block outputs a detect signal (Fig. 1, items 34 and 44) that asserts when it is powered up and ready for use. Coupled to each interface is a power routing block (Fig. 1, item 60) that converts power from the interface block that is energized, to an internal voltage that is used by the remainder of the circuit (column 2, lines 33-39; CardVcc of Fig. 1). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the power routing block of Spencer as a means for providing power to the memory card through the interface to which the memory card was connected.

One of ordinary skill in the art would have found it obvious that including a power routing block, of Spencer, in the dual interface memory card of Yao, allows a memory card to receive power from an attached device rather then having to provide its own limited supply power source, thus saving internal battery life of a memory card.

20. Claims 2 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu as applied to claim 1 above, and further in view of Yao.

For claims 2 and 7-8:

As previously discussed above, Liu teaches a silicon card with bi-interface comprising: a silicon card and its converting device, wherein the silicon card has

- a first transfer interface (Fig. 1, 14; [0020]) and
- circuit broad having
    - microcontroller (Fig. 1, 22; [0020]) and erasable memory media (Fig. 1, 16; [0020]),
    - a first bus interface is provided in the microcontroller (Fig. 1, 28; [0021]),
    - a slot for receiving the silicon card ([0032] describes the process completed when the Flash memory card (Fig. 1, 10) is inserted into the appropriate slot) and
    - a second transfer interface for connecting with peripheral device (Fig. 1, 12; [0020]) are provided in the converting device).
- another second bus interface circuit (Fig. 1, 30; [0022]) and

an interface detecting control and switching circuit are provided in the microcontroller of the silicon card, the interface detecting control and switching circuit has the function of allowing the

microcontroller to automatically detect and determine that if the system supports either the first transfer interface or the second transfer interface so that the data can be stored and read in the erasable memory media (Fig. 1, 20; [0024-0030]). Liu also teaches a temporary store unit (Fig. 1, 26; [0031]), power convert circuit (Fig. 1-2, 18, [0024]), and control store and read interface program code store memory media in the microcontroller [0031]. Liu further teaches the first transfer interface and first bus interface are compliant with the compact flash (CF) specification but does not teach the first transfer interface or first bus interface complying to the memory stick (MS) specification.

Yao has been previously shown to teach a MS (col. 4, ll. 30-36) silicon card with bi-interface comprising: a silicon card and its converting device, wherein the silicon card has

- a first transfer interface (Fig. 1, 102; col. 2, ll. 45-57; Fig. 3, "Host Interface 143"; col. 3, ll. 6-10) and
- circuit broad having
    - microcontroller (Fig. 1-2, 10) and erasable memory media (Fig. 1-2, 20),
    - a first bus interface is provided in the microcontroller (Fig. 2, 14; col. 2, ll. 58-63),
    - a slot for receiving the silicon card (Fig. 3, 30; col. 3, ll. 33-48) and
    - a second transfer interface for connecting with peripheral device (Fig. 1, 101; col. 2, ll. 45-57; Fig. 3, 133; col. 3, ll. 1-5) are provided in the converting device (Fig. 4).
- another second bus interface circuit (Fig. 2, 13; col. 2, ll. 58-63) and

an interface detecting control and switching circuit are provided in the microcontroller of the silicon card, the interface detecting control and switching circuit has the function of allowing the microcontroller to automatically detect and determine that if the system supports either the first transfer interface or the second transfer interface so that the data can be stored and read in the erasable memory media (col. 3, ll. 12-26). Furthermore Yao teaches the dual-interface memory card of his invention is applicable to STONE card, Smart Media card, MMC card, Memory Stick card, and Compact Flash card specification (col. 4, ll. 30-36).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the double interface compact flash card of Liu such that the card is compliant with the Memory Stick specification such that achieved invention allows for broader applicability in the marketplace.

For claim 6:

With the respect to the 35 USC § 103(a) rejection of claim 2 above, the Examiner has shown that it would have been obvious to modify the double interface compact flash card of Liu such that the card is compliant with the Memory Stick specification such that achieved invention allows for broader applicability in the marketplace (col. 4, ll. 30-36). As the applicant is aware, the Memory Stick specification has set forth the use of signal ports/pins CLK, SCLK, SDIO, Reserved 1, and Reversed 2 for every device compliant with the MS specification. Therefore the combination of Liu in view of Yao (as discussed with regards to claims 2 and 7-8 above)

inherently teaches the use of signal ports/pins CLK, SCLK, SDIO, Reserved 1, and Reversed 2 as recited in claim 6 of the instant application.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hill (US006779734B2) : Disclose a smart card with two interfaces.

Yen (US006744634B2) : Disclose a dual interface memory card which connects to a host interface and a USB slot on a computer.

Kobayashi(US006088755A): Disclose a dual interface flash memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

RMS

PAUL R. MYERS
PRIMARY EXAMINER